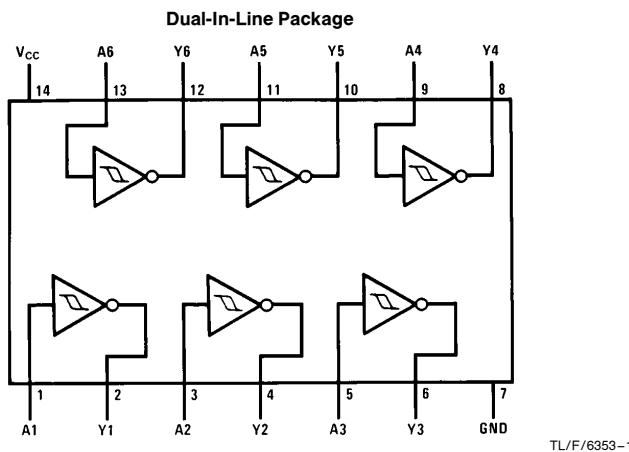


54LS14/DM74LS14 Hex Inverters with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram



Order Number 54LS14DMQB, 54LS14FMQB,
 54LS14LMQB, DM74LS14M or DM74LS14N
 See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$Y = \bar{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54LS14			DM74LS14			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.6	2.0	1.4	1.6	1.9	V
V _{T−}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.8	1.1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I _{OH}	High Level Output Current			−0.4			−0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

 over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −18 mA				−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max	54LS	2.5	3.4		V
			DM74	2.7	3.4		
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min	54LS		0.25	0.4	V
			DM74		0.35	0.5	
		V _{CC} = Min, I _{OL} = 4 mA	DM74		0.25	0.4	
I _{T+}	Input Current at Positive-Going Threshold	V _{CC} = 5V, V _I = V _{T+}	DM74		−0.14		mA
I _{T−}	Input Current at Negative-Going Threshold	V _{CC} = 5V, V _I = V _{T−}	DM74		−0.18		mA
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V	DM74			0.1	mA
		V _{CC} = Max, V _I = 10.0V	54LS				
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V				20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V				−0.4	mA
I _{os}	Short Circuit Output Current	V _{CC} = Max (Note 3)	54LS	−20		−100	mA
			DM74	−20		−100	
I _{CCH}	Supply Current with Outputs High	V _{CC} = Max			8.6	16	mA
I _{CCL}	Supply Current with Outputs Low	V _{CC} = Max			12	21	mA

Note 1: V_{CC} = 5V.

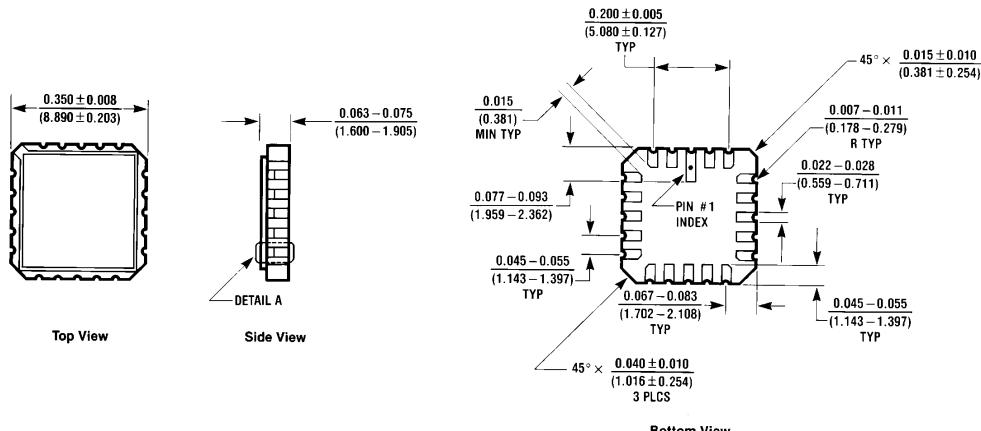
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$ (See Section 1 for Test Waveforms and Output Load)

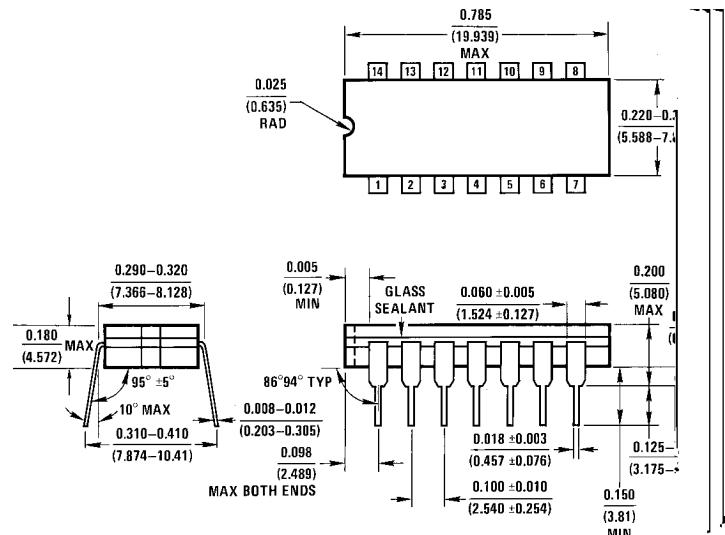
Symbol	Parameter	$R_L = 2\text{ k}\Omega$				Units	
		$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$			
		Min	Max	Min	Max		
t_{PLH}	Propagation Delay Time Low to High Level Output	5	22	8	25	ns	
t_{PHL}	Propagation Delay Time High to Low Level Output	5	22	10	33	ns	

Physical Dimensions



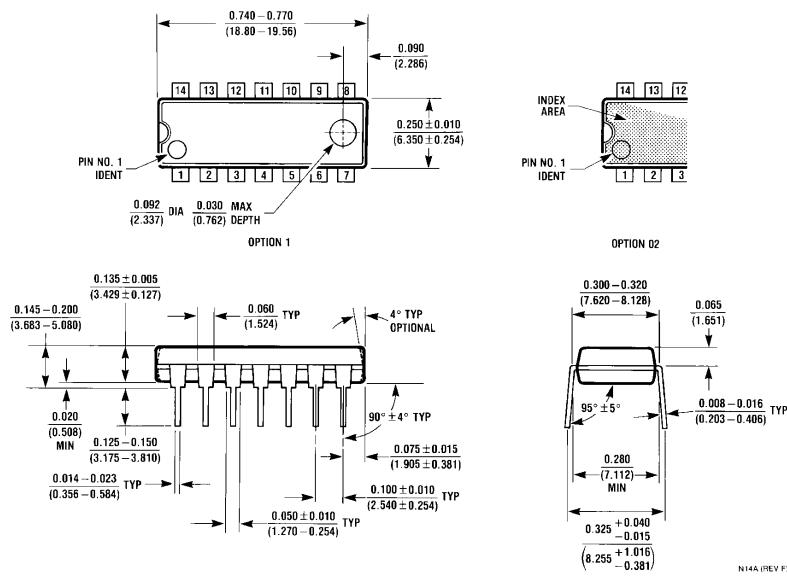
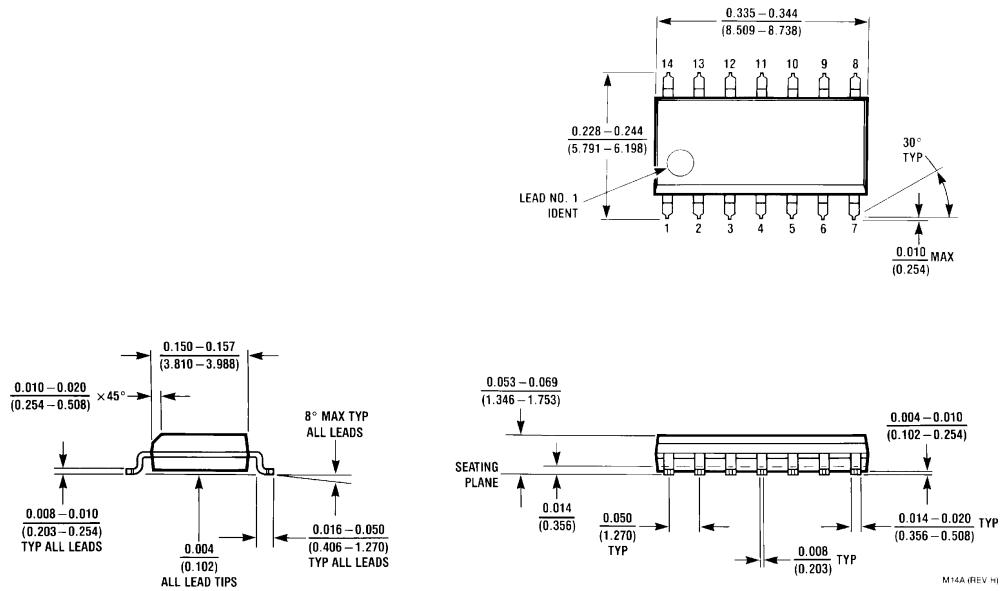
**Ceramic Leadless Chip Carrier (E)
Order Number 54LS14LMQB
NS Package Number E20A**

E20A (REV D)

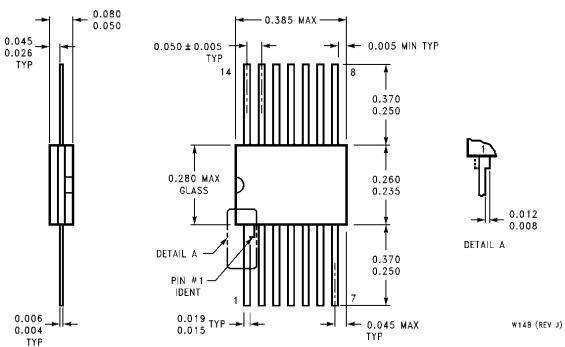


**14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS14DMQB
NS Package Number J14A**

Physical Dimensions inches (millimeters) (Continued)



Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS14FMQB
NS Package Number W14B

LIFE SUPPORT POLICY

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